

CLAIMS

What is claimed is:

- 1 1. An apparatus comprising:
2 a slave access circuit coupled to one of P slave devices and K slave
3 buses to provide access to the one of the P slave devices from one of N
4 master processors via a system bus controller, the K slave buses being
5 configured to couple to the P slave devices, the system bus controller
6 dynamically mapping address spaces of the P slave devices; and
7 a slave bus decoder coupled to the slave access circuit to enable the
8 one of the P slave devices to connect to one of the K slave buses when the
9 one of the P slave devices is addressed by the one of the N master
10 processors; the slave bus decoder being controlled by the system bus
11 controller.

- 1 2. The apparatus of claim 1 wherein the slave access circuit
2 comprises:
3 K bus buffers coupled to the K slave buses to buffer bus signals
4 corresponding to access signals to the one of the P slave devices, the K bus
5 buffers being enabled by the slave bus decoder.

- 1 3. The apparatus of claim 2 wherein each of the K bus buffers is
2 connected to each of the K slave buses.

1 4. An apparatus comprising:
2 an arbiter to arbitrate access requests from N master processors via
3 N master buses, the arbiter generating arbitration signals;
4 a mapping circuit to store mapping information to dynamically map
5 an address space of P slave devices coupled to K slave buses based on the
6 arbitration signals; and
7 a switching circuit coupled to the arbiter and the mapping circuit to
8 connect the N master buses to K slave buses based on the arbitration
9 signals and the mapping information.

1 5. The apparatus of claim 4 further comprising:
2 a slave access decoder coupled to the arbiter and the N master
3 processors to decode addresses issued by the N master processors, the
4 slave access decoder generating control signals to P slave interface
5 circuits, each of the P slave interface circuits being connected to each of
6 the P slave devices.

1 6. The apparatus of claim 5 wherein the mapping information is
2 provided by a supervisor processor.

1 7. The apparatus of claim 4 wherein the mapping information is
2 accessible to the N master processors.

1 8. A method comprising:

2 providing access to one of the P slave devices from one of N
3 master processors via a system bus controller and K slave buses, the K
4 slave buses being configured to couple to the P slave devices;

5 dynamically mapping address spaces of the P slave devices by the
6 bus controller;

7 enabling the one of the P slave devices to connect to one of the K
8 slave buses by a slave bus decoder when the one of the P slave devices is
9 addressed by the one of the N master processors; and

10 controlling the slave bus decoder by the system bus controller.

1 9. The method of claim 8 wherein providing access comprises:

2 buffering bus signals corresponding to access signals to the one of
3 the P slave devices by K bus buffers; and

4 enabling the K bus buffers by the slave bus decoder.

1 10. The method of claim 9 wherein buffering the bus signals
2 comprises:

3 connecting each of the K bus buffers to each of the K slave buses.

1 11. An method comprising:

2 arbitrating access requests from N master processors via N master
3 buses by an arbiter, the arbiter generating arbitration signals;

4 storing mapping information in a mapping circuit to dynamically
5 map an address space of P slave devices coupled to K slave buses based on
6 the arbitration signals; and

7 connecting the N master buses to K slave buses based on the
8 arbitration signals and the mapping information.

1 12. The method of claim 11 further comprising:

2 decoding addresses issued by the N master processors by a slave
3 access decoder;

4 generating control signals to P slave interface circuits by the slave
5 access decoder, each of the P slave interface circuits being connected to
6 each of the P slave devices.

1 13. The method of claim 12 wherein the mapping information is
2 provided by a supervisor processor.

1 14. The method of claim 11 wherein the mapping information is
2 accessible to the N master processors.

1 15. A system comprising:

2 a bus controller coupled to N bus masters and K slave buses;

3 P slave devices; and

4 P slave interface circuits coupled to the P slave devices and the K
5 slave buses, each of the P slave interface circuits comprising:

6 a slave access circuit coupled to one of the P slave devices
7 and the K slave buses to provide access to the one of the P slave
8 devices from one of the N master processors via the system bus
9 controller, the K slave buses being configured to couple to the P
10 slave devices, the system bus controller dynamically mapping
11 address spaces of the P slave devices, and

12 a slave bus decoder coupled to the slave access circuit to
13 enable the one of the P slave devices to connect to one of the K
14 slave buses when the one of the P slave devices is addressed by the
15 one of the N master processors, the slave bus decoder being
16 controlled by the system bus controller.

1 16. The system of claim 15 wherein the slave access circuit comprises:

2 K bus buffers coupled to the K slave buses to buffer bus signals
3 corresponding to access signals to the one of the P slave devices, the K bus
4 buffers being enabled by the slave bus decoder.

1 17. The system of claim 16 wherein each of the K bus buffers is
2 connected to each of the K slave buses.

1 18. A system comprising:

2 N bus masters having N master buses;

3 P slave devices coupled to K slave buses; and

4 A system bus controller coupled to the N bus masters and the K
5 slave buses, the bus controller comprising:

6 an arbiter to arbitrate access requests from the N master
7 processors via the N master buses, the arbiter generating arbitration
8 signals,

9 a mapping circuit to store mapping information to
10 dynamically map an address space of P slave devices coupled to K
11 slave buses based on the arbitration signals, and

12 a switching circuit coupled to the arbiter and the mapping
13 circuit to connect the N master buses to K slave buses based on the
14 arbitration signals and the mapping information.

1 19. The system of claim 18 wherein the system bus controller further
2 comprising:

3 a slave access decoder coupled to the arbiter and the N master processors
4 to decode addresses issued by the N master processors, the slave access decoder
5 generating control signals to P slave interface circuits, each of the P slave interface
6 circuits being connected to each of the P slave devices.

1 20. The system of claim 19 wherein the mapping information is
2 provided by a supervisor processor.

1 21. The system of claim 18 wherein the mapping information is
2 accessible to the N master processors.